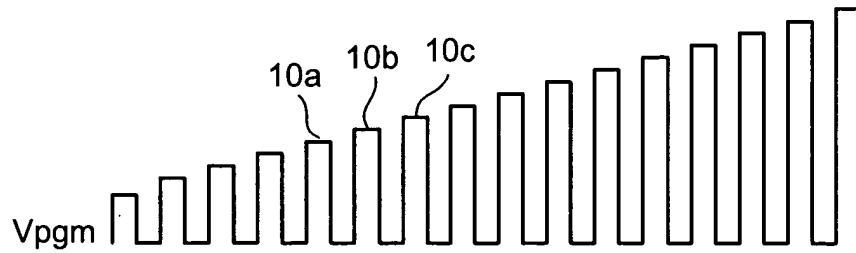


Fig. 1



of cells

Fig. 2

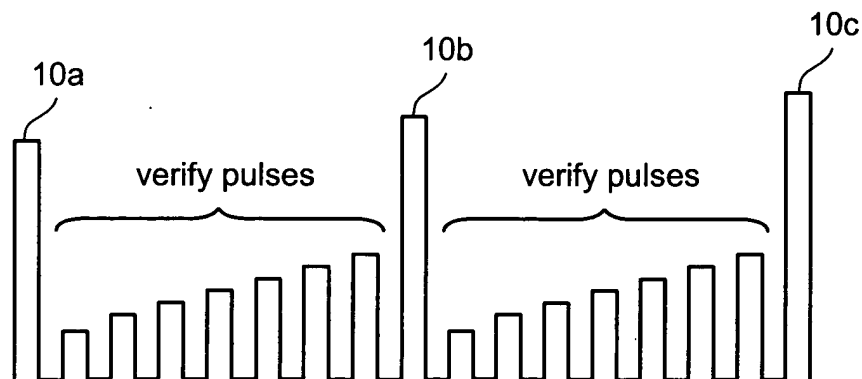
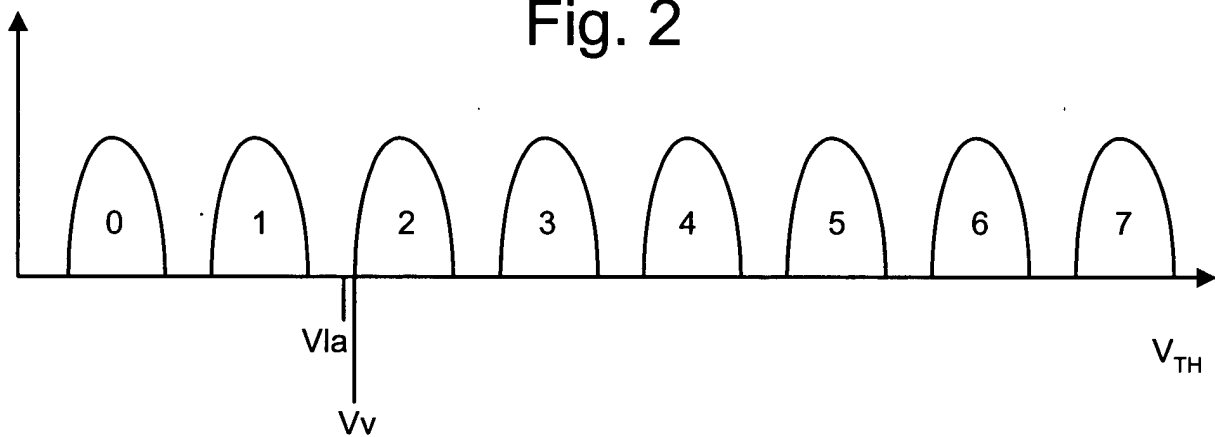


Fig. 3

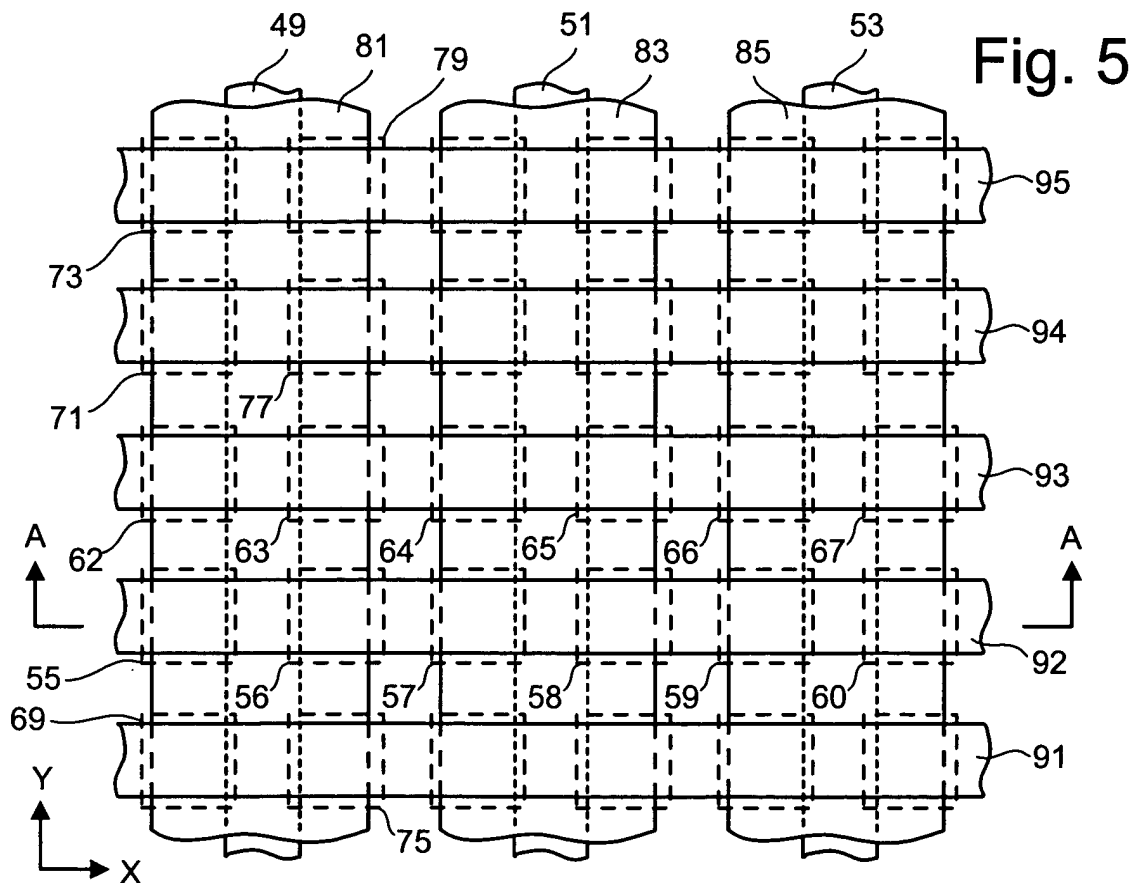
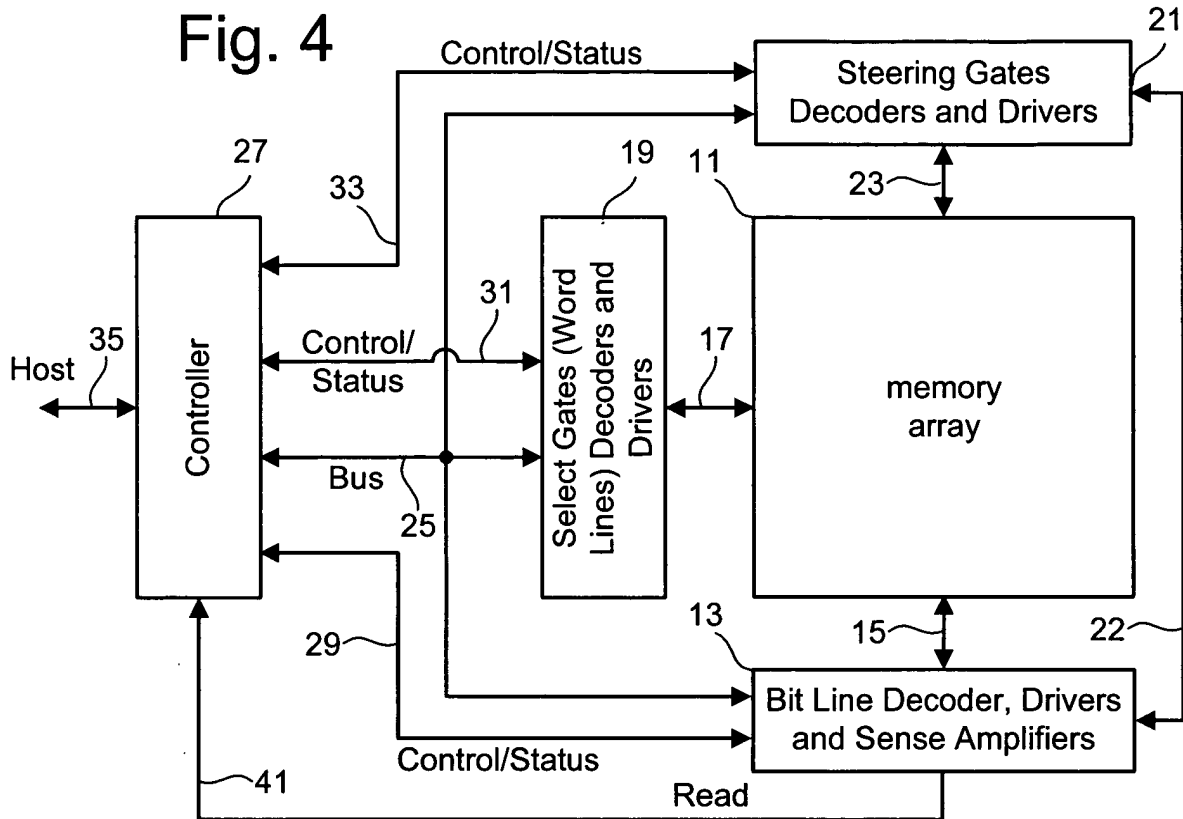


Fig. 6

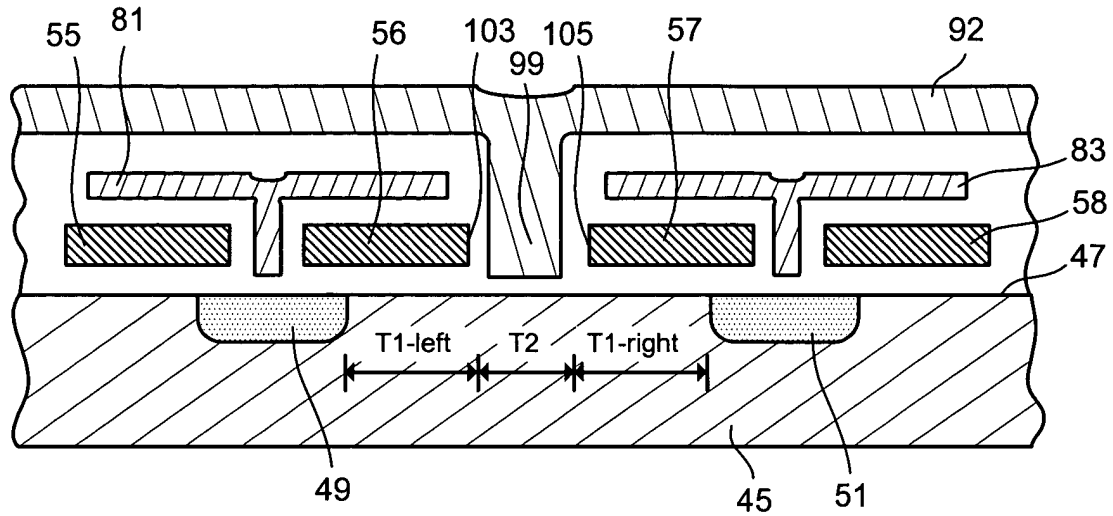
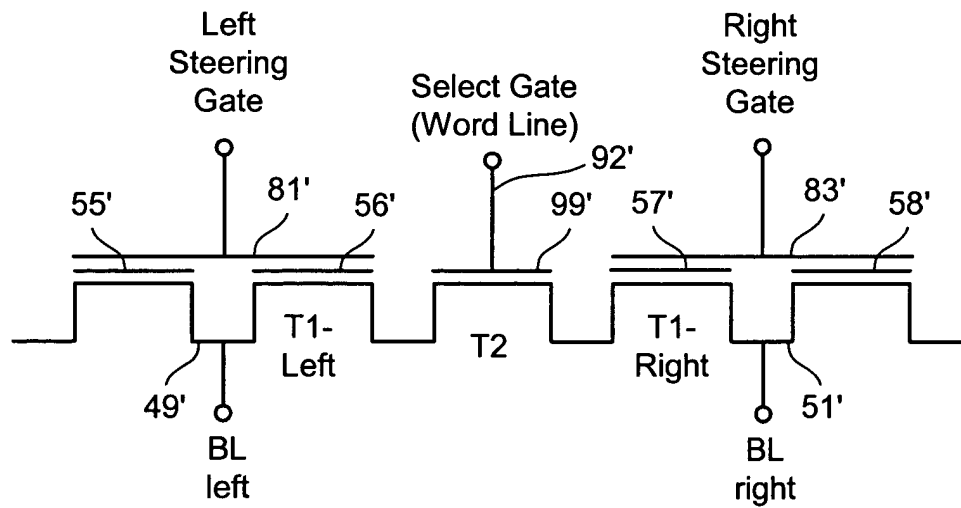


Fig. 7



Title: VARIABLE CURRENT SINKING FOR COURSE/FINE PROGRAMMING OF NON-VOLATILE MEMORY

Applicants: Guterman, et al.

Docket No.:

SAND-01015US0

Appl. No.: Unknown

Atty:

Burt Magen

Filing Date: January 27, 2004

Phone:

(415) 369-9660

Express Mail No.: EV 391 867 391 US

Fig. 8

FUNCTION BEING PERFORMED ON CELL	SELECT GATE (WORD LINE)	LEFT BIT LINE (BL - LEFT)	LEFT STEERING GATE	RIGHT STEERING GATE	RIGHT BIT LINE (BL-RIGHT)
(1) UNSELECTED ROW (2) ERASE (TO WORD LINE) (3) READ LEFT FLOATING GATE (4) READ RIGHT FLOATING GATE (5) PROGRAM LEFT FLOATING GATE (6) PROGRAM RIGHT FLOATING GATE (7) NO PROGRAM IN SELECTED ROW	0 V_E V_{SR} V_{SR} V_{SP} V_{SP} V_{SP}	X 5 0 1 5 0 0 5	X 0 V_M V_{BR} V_P V_{BP} X X	X 0 V_{BR} V_M V_{BP} V_P X X	X 5 1 0 0 5 0 5
(8) ERASE (TO CHANNEL) [WITH VOLTAGES OF BOTH THE p-well AND n-well EQUAL TO V_E , AND THE SUBSTRATE AT ZERO VOLTS]	V_{SE}	FLOAT	0	0	FLOAT

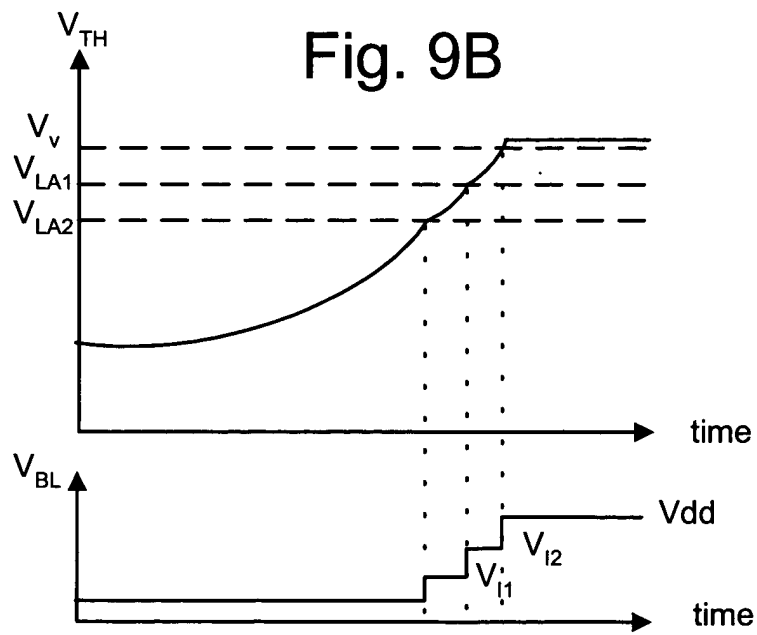
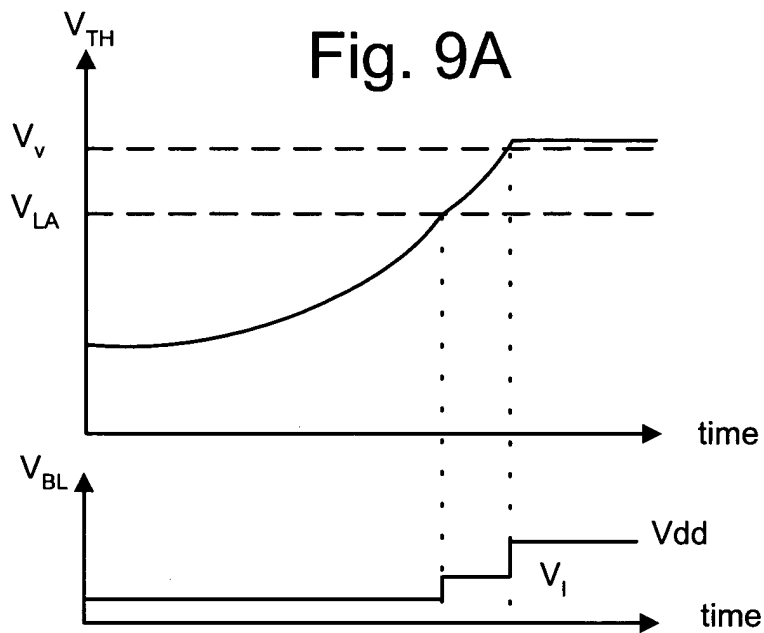
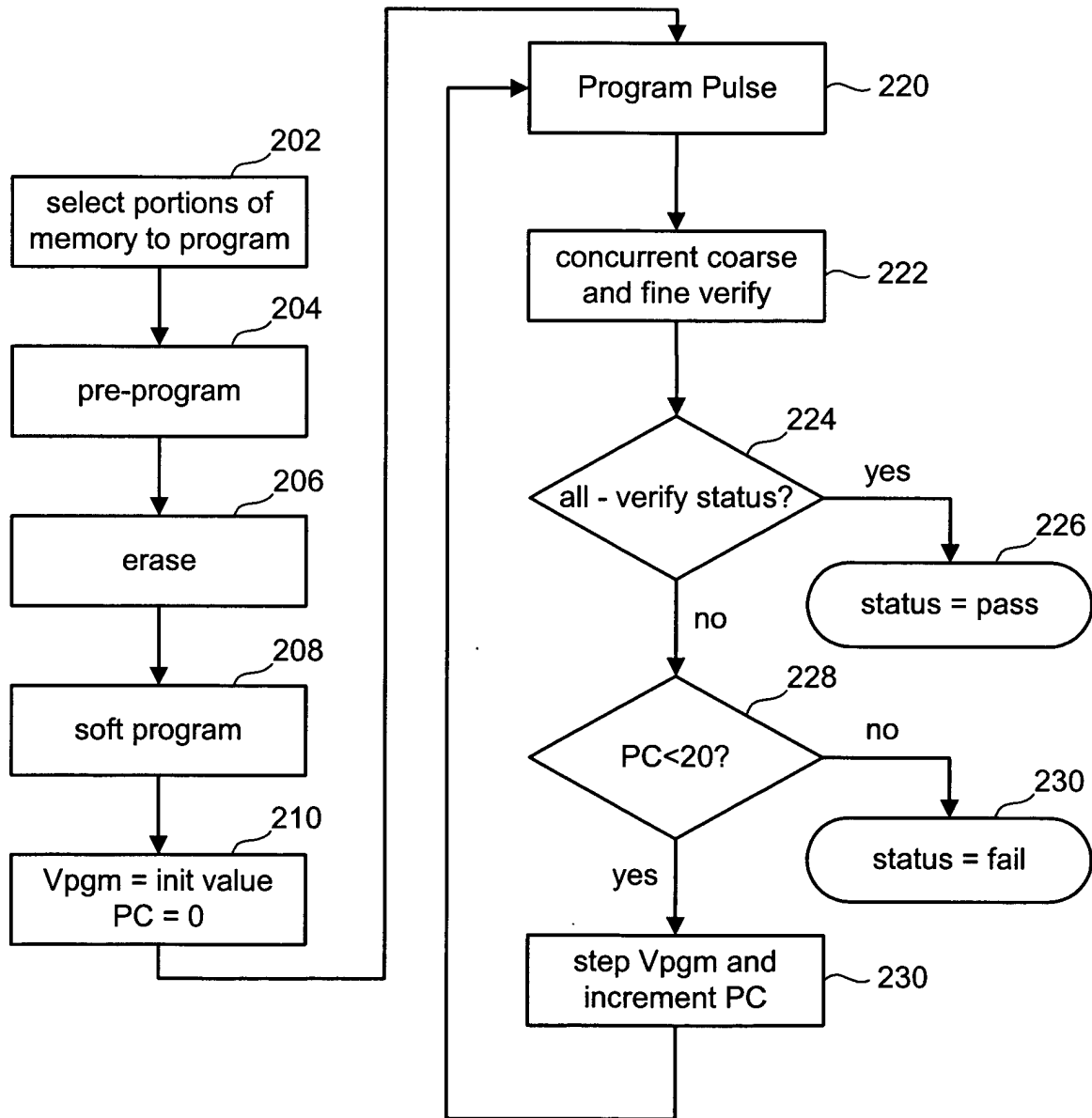


Fig. 10



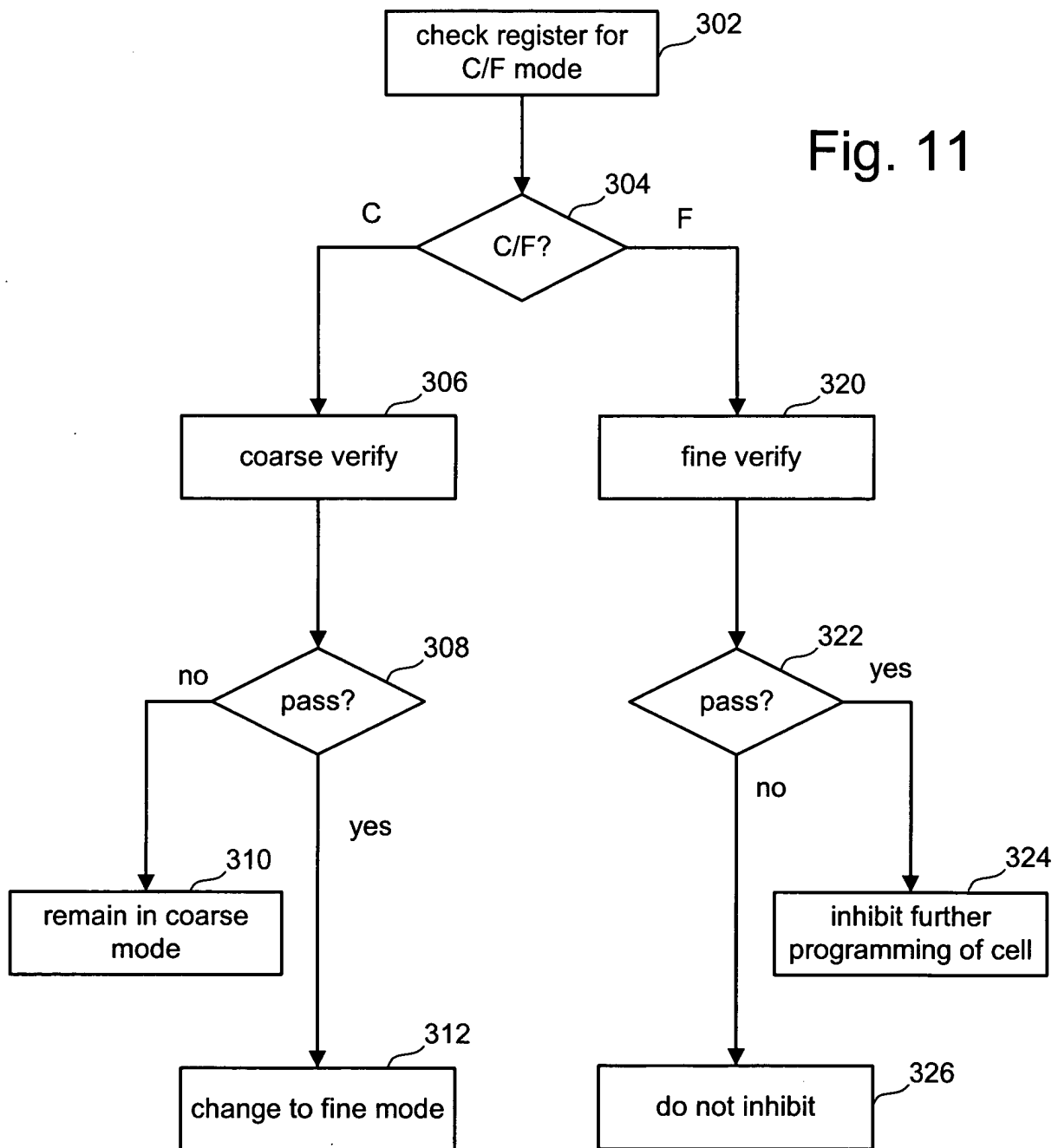


Fig. 12

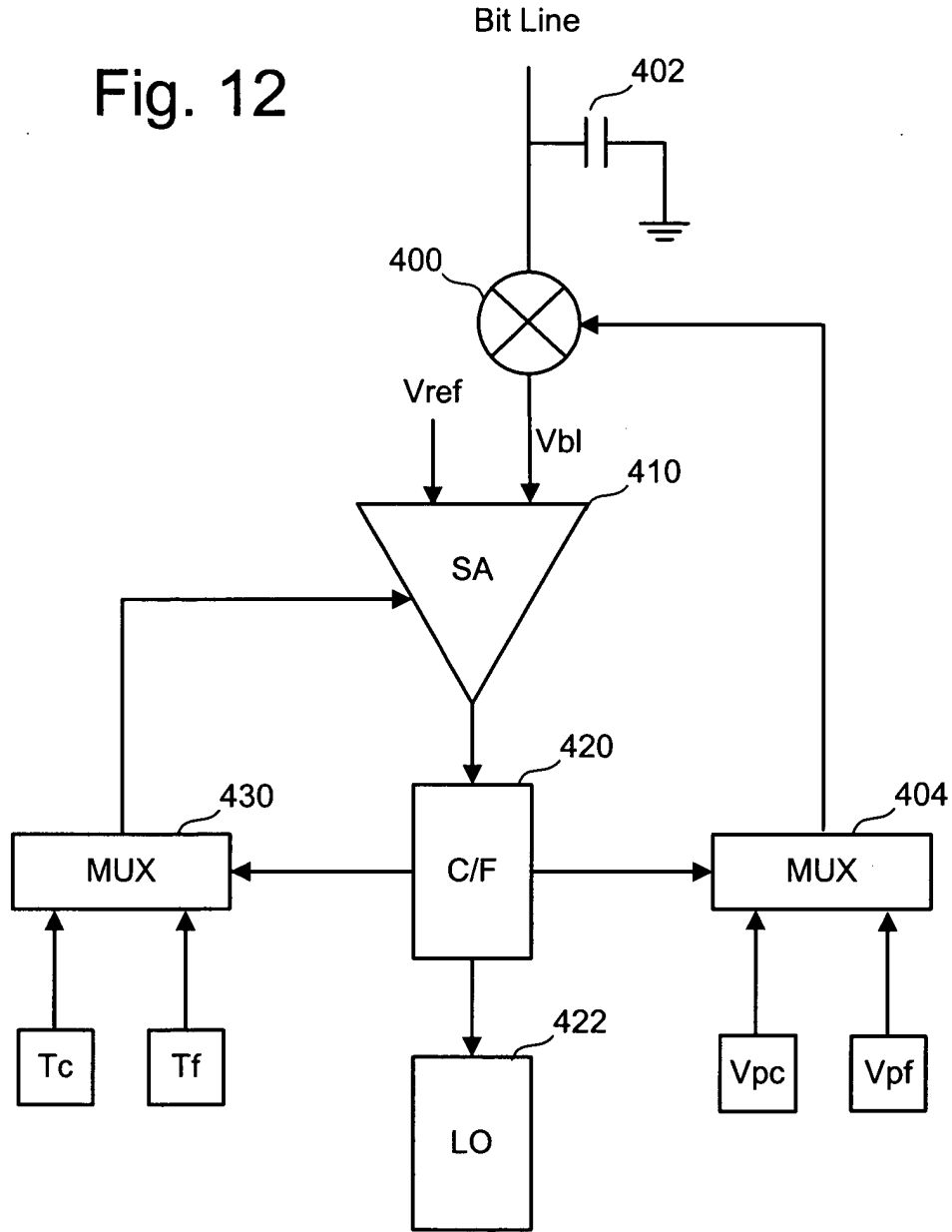


Fig. 13

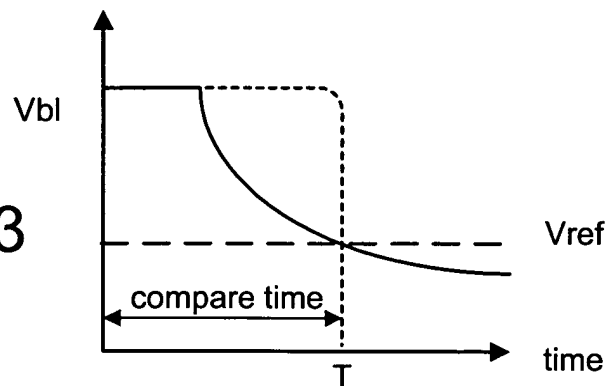


Fig. 14

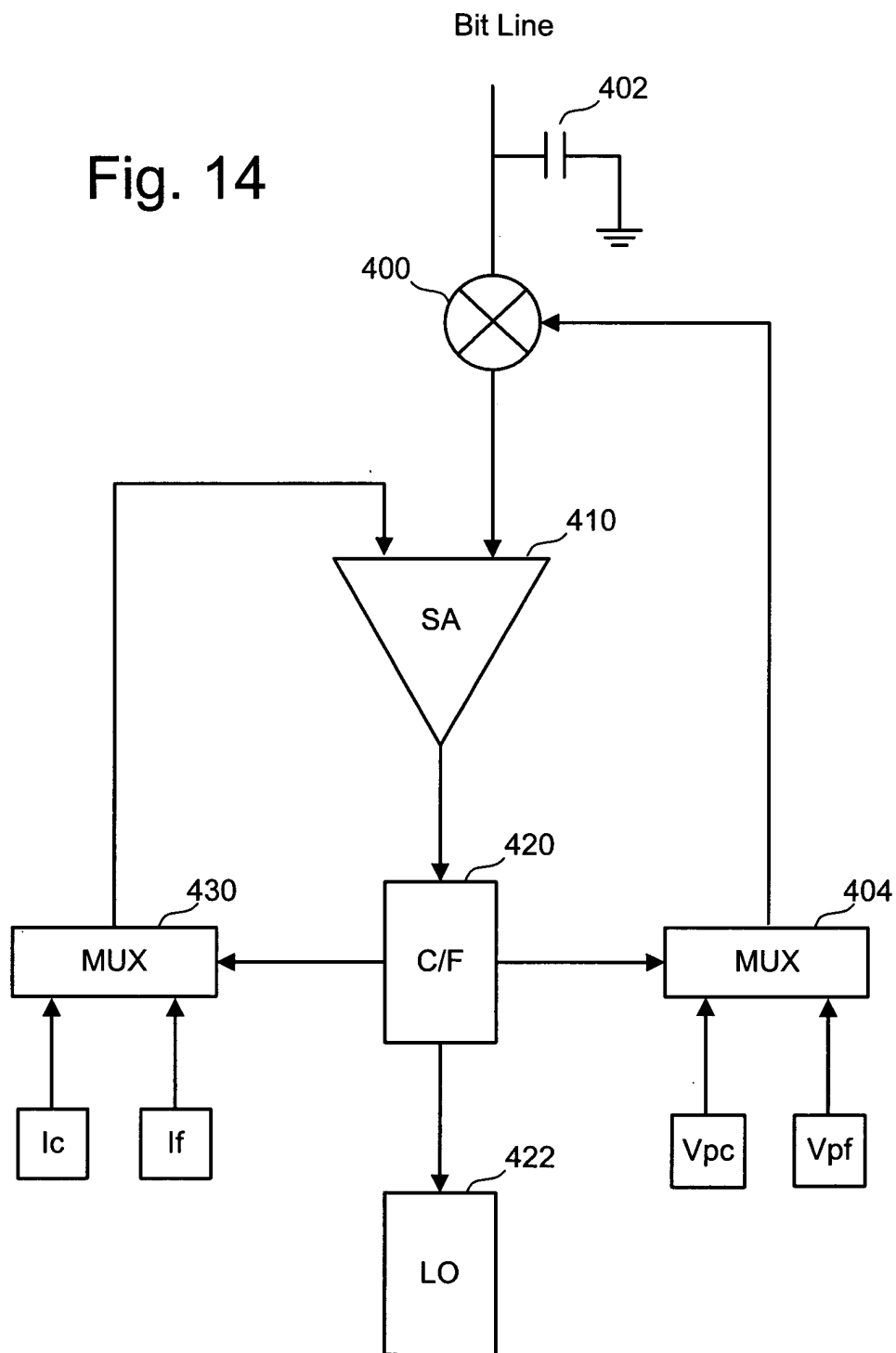


Fig. 15

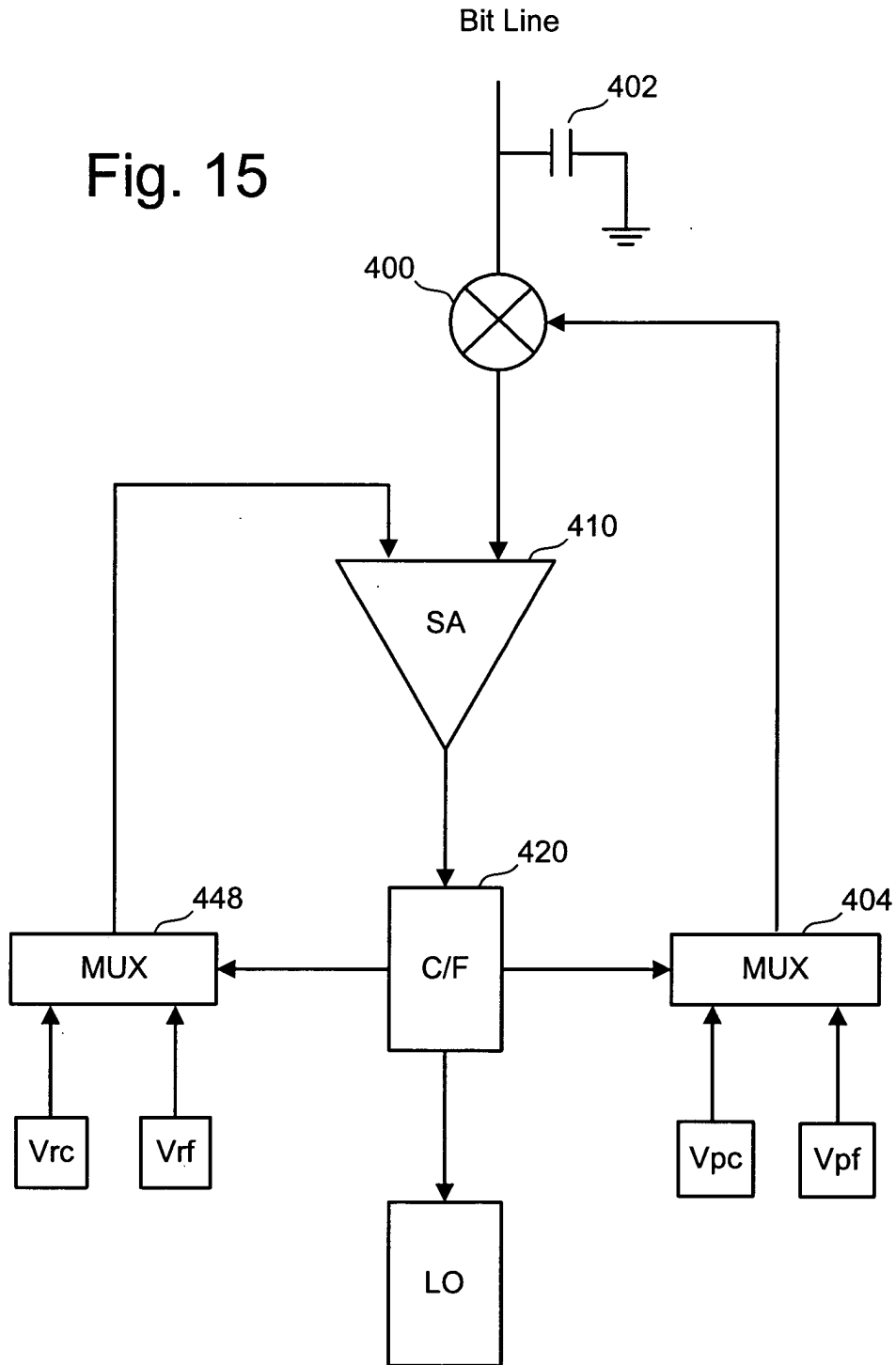
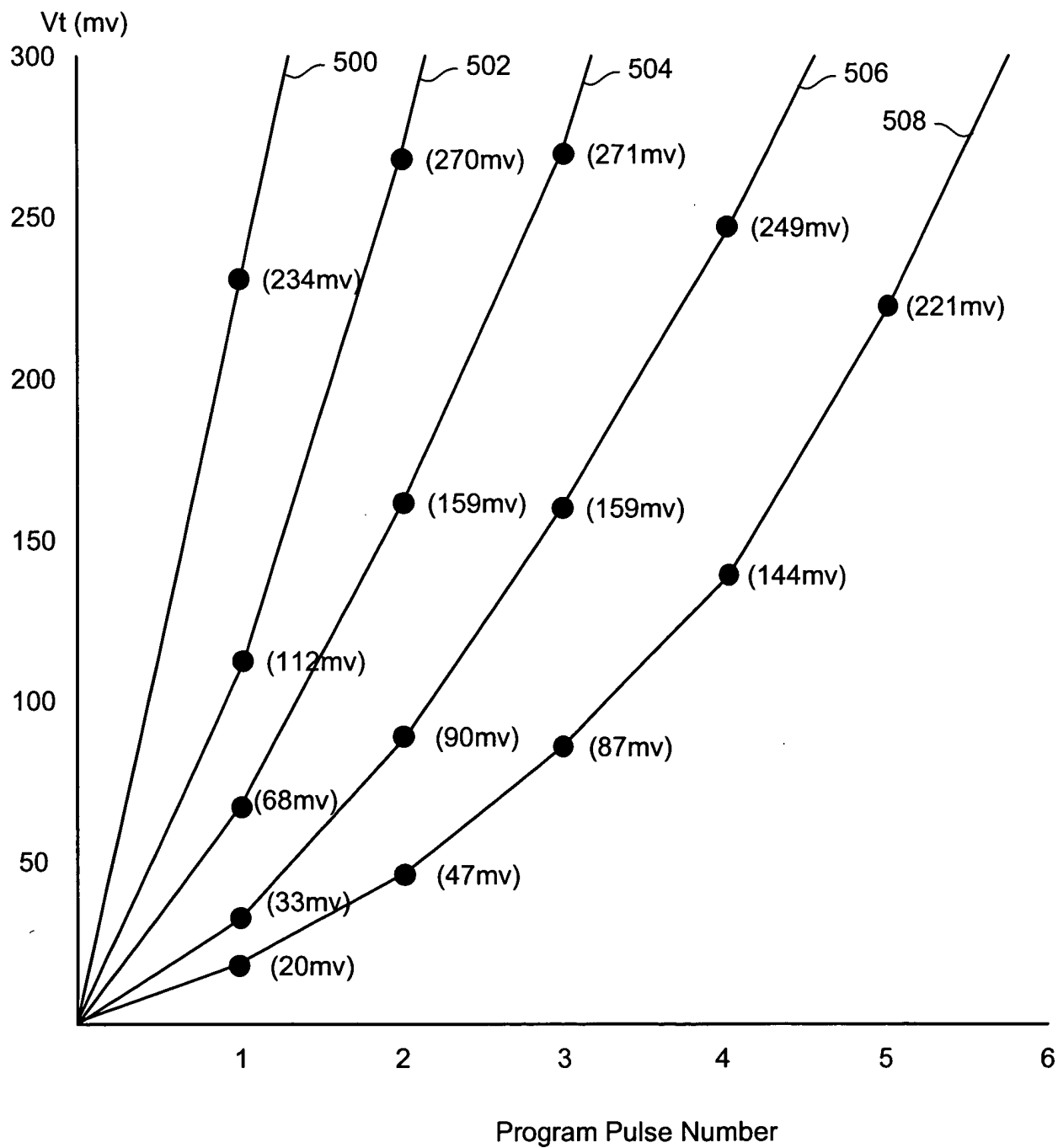


Fig. 16



[illegible]

The diagram illustrates a memory cell array with three columns of cells. The first column is labeled 'Left Steering Gate' and contains a transistor 'T1-Left' with gate 49' and source/drain regions 55' and 56'. The second column is labeled 'Select Gate (Word Line)' and contains a transistor 'T2' with gate 92' and source/drain regions 81' and 99'. The third column is labeled 'Right Steering Gate' and contains a transistor 'T1-Right' with gate 51' and source/drain regions 57' and 58'. The output of the 'T1-Right' transistor is connected to a crossbar array (620) which is part of a larger circuit including a C/F block (420) and two output nodes (622 and 624) connected to ground.

Fig. 19

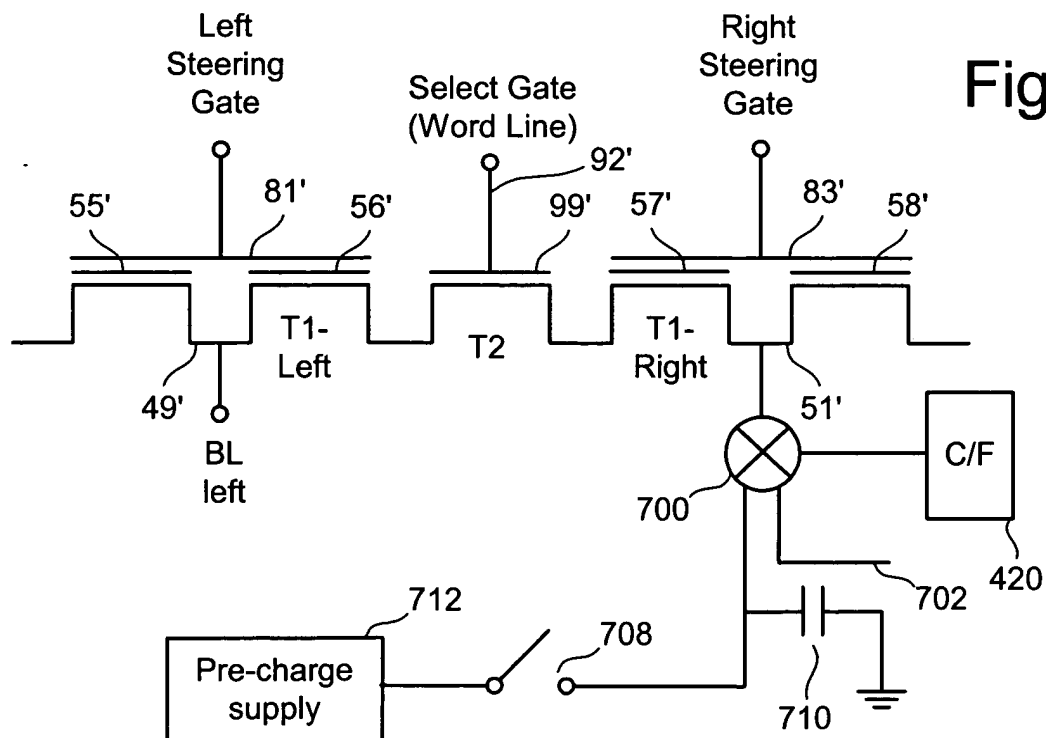
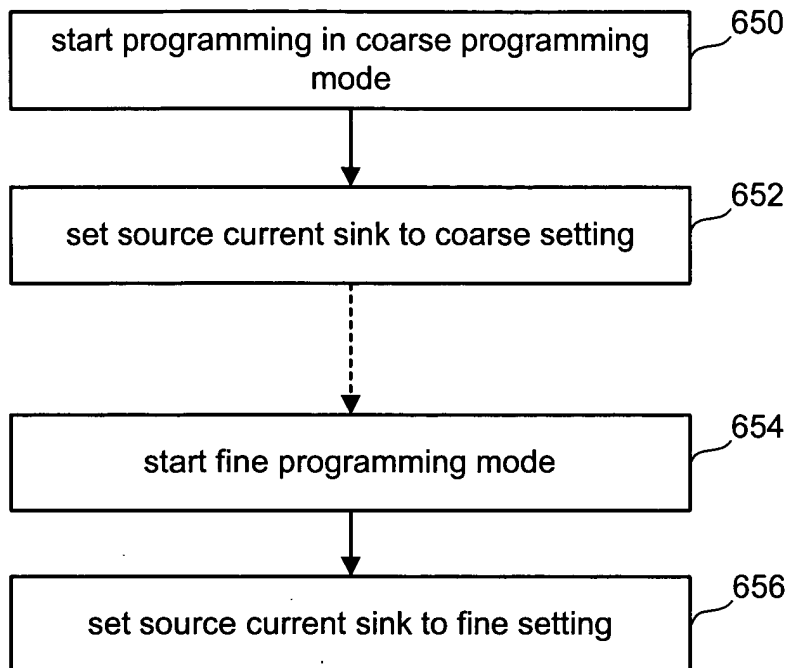


Fig. 20

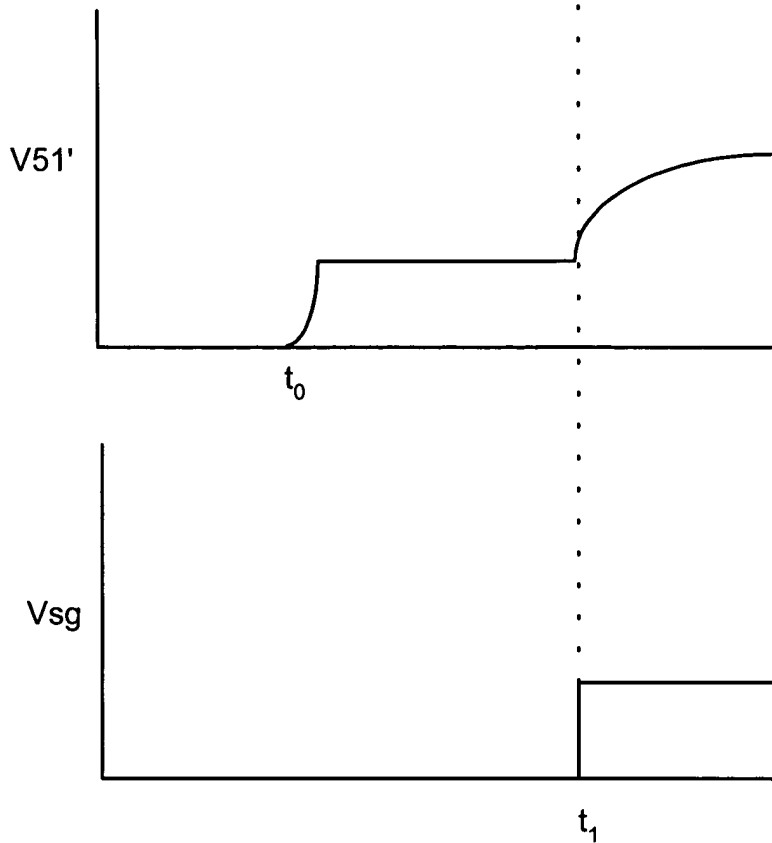


Fig. 21

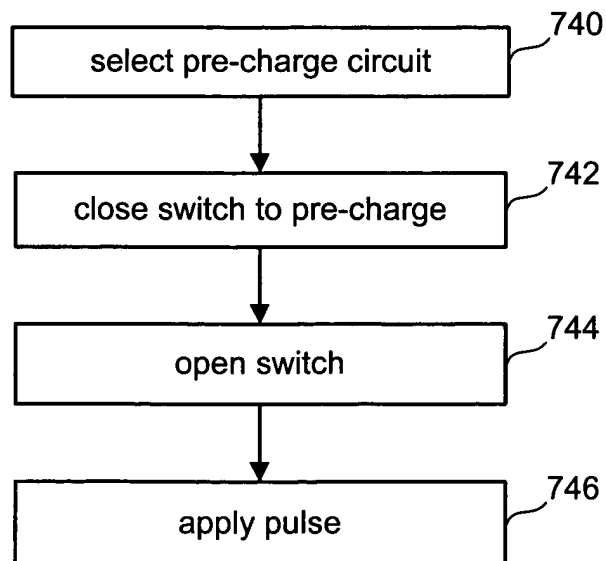


Fig. 22

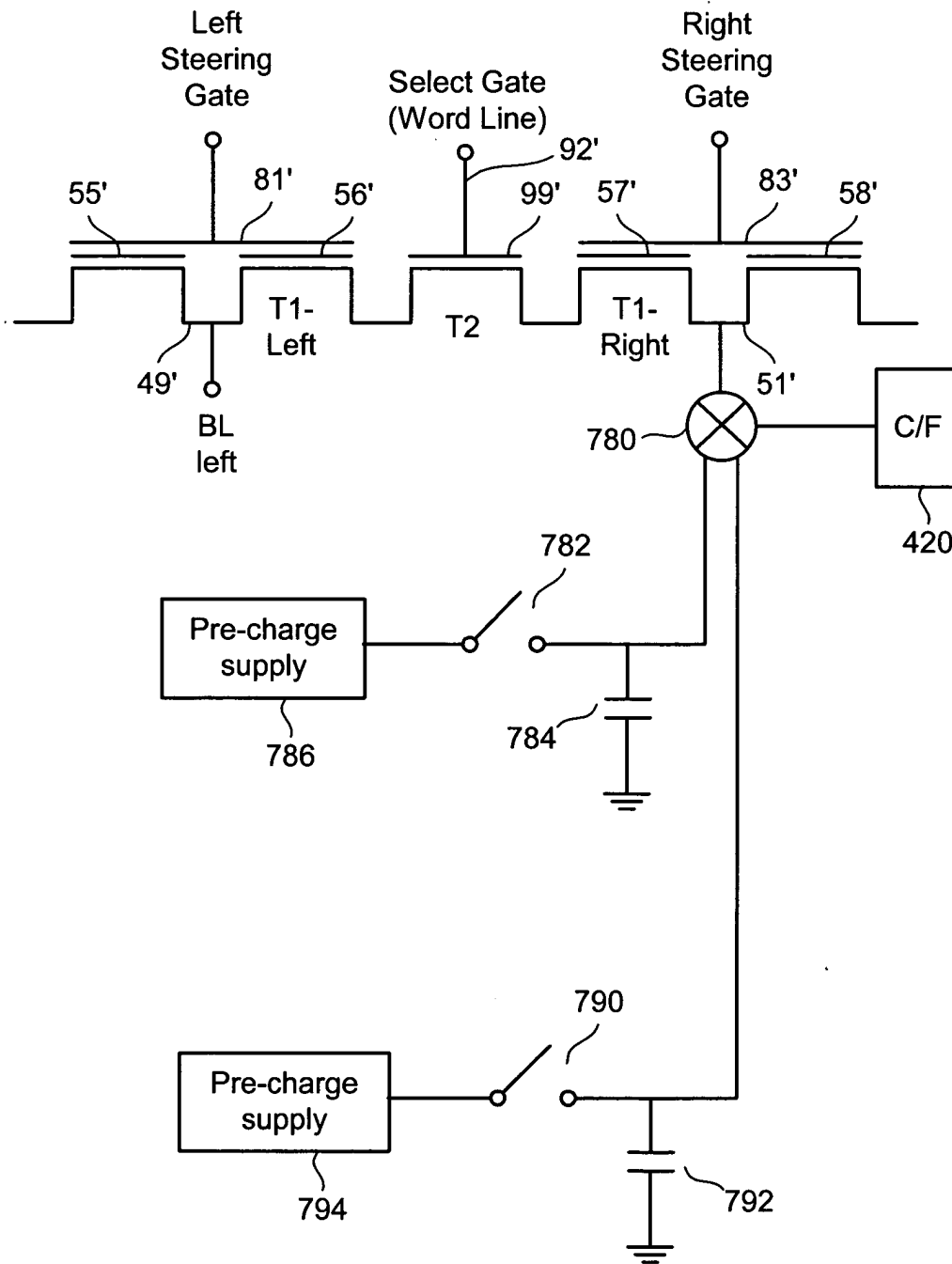


Fig. 23

